Amendments to the Specification:

Please replace paragraph **[0015]** with the following amended paragraph:

--**[0015]** Figures 1 through 3 illustrate a method for forming a tunnel oxide window for a conventional EEPROM device. As shown, the conventional method begins by providing a substrate [[101,]] 100, which includes a surface region 101. The surface region is provided between isolation regions 103. The isolation regions are often formed using local oxidation of silicon, commonly called LOCOS. The method forms a dielectric layer 201 overlying the surface region. The dielectric layer is often patterned to form a tunnel window 205. The tunnel window is a region that has a thickness that is thinner than surrounding dielectric layer regions. A gate electrode layer 207 is often formed overlying the dielectric layer. Preferably, the gate electrode is a floating gate for EEPROM devices. Referring to Figure 3, tunnel window 205 has a square confirmation, which is often formed using masking and etching techniques. Also shown is select gate 303 and source line ~~301 the~~ 301. The floating gate 207 is formed overlying the dielectric layer, which is formed overlying the surface region. Field isolation oxide layers 103 are also shown. Certain limitations exist with this conventional EEPROM device. A width L' and length L of the tunnel window can be provided only up to a certain dimension. That is, conventional tunnel windows can be 0.45 to about 0.8 microns in size, but often cannot be smaller using conventional masking and etching techniques. These and other limitations of conventional EEPROM devices can be found throughout the present specification. Further details of overcoming certain limitations of these conventional EEPROM devices are found throughout the present specification and more particularly below.--

Please replace paragraph **[0018]** with the following amended paragraph:

--**[0018]** Figures 4 through 8 illustrate a method for forming an EEPROM device according to an embodiment of the present invention. These diagrams are merely examples, which should not unduly limit the scope of the claims herein. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. In a specific embodiment, the invention provides a method for forming an EEPROM integrated circuit structure. As shown, the method

begins by providing a substrate [[401]] 400 including a surface region [[400,]] 401, which is provided within a first cell region. Other cell regions numbered from 2 through N (not shown) are also included. The substrate is [[a]] made of a suitable material such as silicon, silicon on insulator, or epitaxial silicon. The surface region is provided between field isolation oxide regions 403. The field isolation oxide regions can be formed using any suitable techniques such as Local Oxidation of Silicon, commonly called LOCOS, or Shallow Trench Isolation, often called STI. Other isolation techniques can also be used.--

Please replace paragraph **[0019]** with the following amended paragraph:

--**[0019]** The method also includes forming a gate dielectric layer of first thickness overlying the surface region of the substrate. ~~region.~~ The gate dielectric layer is often a high quality thermal oxide, silicon oxynitride, or silicon nitride, depending upon the application. The method also includes patterning the gate dielectric layer to form a plurality of stripes. Each of the stripes is characterized by a second thickness, which is less than the first thickness. Each of the stripes has a predetermined width and a predetermined length that have been formed using a phase shift mask. Preferably, the pre determined width is less than 0.25 microns, which leads to a smaller cell size. At least one 407 of the stripes includes a stripe portion traversing through a portion of the first cell region and other cell regions, which may have other devices. Referring to Figure 6 (see reference letter A' to A, which maps onto the same for Figure 5), which is a ~~topview~~ top view diagram of an expanded view of Figure 5, the device has a select gate 601, which runs along the cell. Field isolation oxide regions 403 are also shown. The stripe portion 407 is also shown. The stripe portion runs through the cell, as well as other cells, which are adjacent to the cell shown. The method also includes forming a floating gate 405 overlying a portion of the gate dielectric layer. As shown, [[as]] a portion of the gate dielectric layer includes the stripe portion traversing through the portion of the gate dielectric layer. A source line 603 is also shown.--